A Novel Unequal Power Divider With General Isolation Topology: Design and Verification

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***Abstract*— In this letter, a novel unequal power divider (PD) with three standard 50-Ω ports is presented. It consists of two transmission line (TL) sections, two resistors, and a general isolation topology (GIT). Through analyzing voltages and currents of each branch, the constraint conditions of such a GIT are newly established. Considering realization of GIT, two types of topologies, i.e., asymmetrical coupled line and cascaded TL, are selected for verification. From the design charts and several design examples, the proposed PD could not only provide high power ratio k^2 with compact size but also independently adjust their fractional bandwidths (S_{11} or S_{32}) with the same power ratio k^2. Finally, an unequal PD with the power ratio $k^2 = 8$ is fabricated, and the measured results meet the simulated results very well.**

***Index Terms*— Compact size, general isolation topology (GIT), high power ratio, standard 50-Ω ports, unequal power divider (PD).**

I. Introduction

UNEQUAL power divider (PD) has been widely used in RF/microwave circuits and systems, which can split the power with different ratios. Many unequal Wilkinson PDs (WPDs) have been developed so far in [1], [2], [3], and [4], where the power ratio between two output ports is determined by the port loads. In order to connect them with other circuits, extra impedance transformers often need to be added at the end of output ports, thus making their overall size very large. For Gysel PDs, unequal power division is reportedly achieved in [5], [6], and [7]. Because the resistors need to be shunt-connected to the ground, their power losses cannot be ignored at all. Moreover, considering the size of miniaturization and loss reduction, unequal PDs to be directly terminated with three standard 50-Ω ports [8], [9], [10] are definitely preferred in many industrial applications.

In this letter, a novel unequal PD with three standard 50-Ω ports is introduced. By analyzing the voltages and currents of each branch, the constraint conditions of general isolation topology (GIT) are newly established. Considering realization of GIT, two types of topologies, i.e., asymmetrical coupled line (ACL) and two cascaded transmission lines (TLs), are selected for verification. Several design examples are provided with different fractional bandwidths (FBWs) and power ratios. One circuit prototype is further fabricated to confirm the theoretical simulation in experiment. Compared with the former works in [1], [2], [3], [4], [5], [6], [7], [8], [9], and [10], three unique advantages can be derived and summarized as: 1) a GIT is newly analyzed under novel constraint conditions; 2) by analyzing the design charts of two cases, ACL in case I is preferred for high power ratio, wide FBW of S_{11}, and compact circuit size; and 3) FBW of S_{11} (or FBW of S_{32}) and power ratio (k^2) can be adjusted independently.

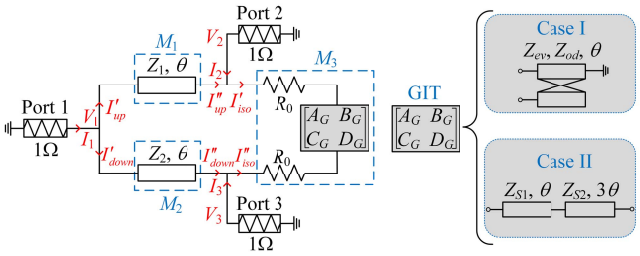

Fig. 1. Schematic of the proposed unequal PD with GIT.

II. Design Equations

Fig. 1 shows the schematic of the proposed unequal PD with GIT, where three terminal load impedances are normalized as 1 Ω. It consists of two TL sections, two resistors (where $R_0 = 1\ \Omega$), and a GIT between two output ports (gray box), where Z_1 and Z_2 are the characteristic impedances of two TLs, and their electrical lengths are denoted as θ. Considering realization of GIT, two types of topologies, i.e., ACL (case I) and two cascaded TLs (case II), are selected for verification in this letter.

In Fig. 1, the three involved *ABCD* matrices, M_1, M_2, and M_3, can be written as

$$[M_1] = \begin{bmatrix} \cos\theta & jZ_1\sin\theta \\ j\sin\theta/Z_1 & \cos\theta \end{bmatrix}$$

$$[M_2] = \begin{bmatrix} \cos\theta & jZ_2\sin\theta \\ j\sin\theta/Z_2 & \cos\theta \end{bmatrix} \tag{1a}$$

$$[M_3] = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} A_G & B_G \\ C_G & D_G \end{bmatrix}\begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} \tag{1b}$$

where V_1, V_2, and V_3 and I_1, I_2, and I_3 are the voltages and currents of three standard 1-Ω ports, respectively. For each part, the input and output currents can be defined as I'_{up}, I''_{up}, I'_{down}, I''_{down}, I'_{iso}, and I''_{iso}, with $I_1 = I'_{\text{up}} + I'_{\text{down}}$, $I_2 = I'_{\text{iso}} - I''_{\text{up}}$,

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and $I_3 = I''_{\text{iso}} - I''_{\text{down}}$. The relationship between the voltages and currents can be expressed as

$$\begin{bmatrix} V_1 \\ I'_{\text{up}} \end{bmatrix} = [M_1] \begin{bmatrix} V_2 \\ I''_{\text{up}} \end{bmatrix}$$
$$\begin{bmatrix} V_1 \\ I'_{\text{down}} \end{bmatrix} = [M_2] \begin{bmatrix} V_3 \\ I''_{\text{down}} \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} V_2 \\ I'_{\text{iso}} \end{bmatrix} = [M_3] \begin{bmatrix} V_3 \\ -I''_{\text{iso}} \end{bmatrix}. \quad (2)$$

For simplification of our calculation, $\theta = 90°$ is defined in this letter. The total admittance matrix $[Y]$ and the S matrix $[S]$ of the proposed unequal PD can be deduced as

$$[Y] = \begin{bmatrix} 0 & j/Z_1 & j/Z_2 \\ j/Z_1 & D_T/B_T & -1/B_T \\ j/Z_2 & -1/B_T & A_T/B_T \end{bmatrix} \quad (3)$$

$$[S] = ([U] + [Y])^{-1}([U] - [Y]) = \frac{1}{Q} \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \quad (4)$$

where $[U]$ is the identity matrix and

$$Q = -Z_1^2(B_T + D_T) - Z_2^2(A_T + B_T) - Z_1^2 Z_2^2(A_T + B_T + C_T + D_T) - 2Z_1 Z_2 \quad (5a)$$
$$S_{11} = Z_1^2(B_T + D_T) + Z_2^2(A_T + B_T) + Z_1^2 Z_2^2(-A_T - B_T + C_T - D_T) + 2Z_1 Z_2 \quad (5b)$$
$$S_{22} = Z_1^2(-B_T + D_T) + Z_2^2(A_T + B_T) + Z_1^2 Z_2^2(-A_T - B_T + C_T + D_T) + 2Z_1 Z_2 \quad (5c)$$
$$S_{33} = Z_1^2(B_T + D_T) + Z_2^2(A_T - B_T) + Z_1^2 Z_2^2(A_T - B_T + C_T - D_T) + 2Z_1 Z_2 \quad (5d)$$
$$S_{23} = S_{32} = 2Z_1 Z_2(B_T - Z_1 Z_2) \quad (5e)$$
$$S_{12} = S_{21} = 2jZ_1 Z_2(Z_1 + A_T Z_2 + B_T Z_2) \quad (5f)$$
$$S_{13} = S_{31} = 2jZ_1 Z_2(Z_2 + B_T Z_1 + D_T Z_1). \quad (5g)$$

For the power splitting and isolation performances of the unequal PD, the following relationship should be satisfied:

$$S_{11} = S_{22} = S_{23} = S_{32} = S_{33} = 0 \quad \text{and} \quad |S_{12}|^2/|S_{13}|^2 = k^2. \quad (6)$$

Finally, all the characteristic impedances and M_3 can be calculated by the following two equations:

$$Z_1 = \sqrt{k^2+1}/k \quad \text{and} \quad Z_2 = \sqrt{k^2+1} \quad (7a)$$
$$A_T = k, \quad B_T = k + 1/k, \quad C_T = 0, \quad \text{and} \quad D_T = 1/k. \quad (7b)$$

For the gray box, the constraint conditions of *ABCD* matrix can be established and simply deduced as

$$A_G = k, \quad B_G = C_G = 0, \quad \text{and} \quad D_G = 1/k. \quad (8)$$

III. Design Examples of the Proposed Unequal PD

To design the proposed unequal PD easily and quickly, a brief flowchart is summarized in Fig. 2. From Fig. 2, −20-dB FBWs of S_{11}, S_{22}, S_{33}, and S_{32} are expressed as FBW_{S11}, FBW_{S22}, FBW_{S33}, and FBW_{S32}, respectively. $\theta_c^{S_{11}}$ (or $\theta_c^{S_{32}}$) is defined as the electrical length at the lower cutoff frequency of S_{11} (or S_{32}), and $\text{RL}^{S_{11}}$ (or $\text{RL}^{S_{32}}$) is the return loss of S_{11} (or S_{32}) at $\theta_c^{S_{11}}$ (or $\theta_c^{S_{32}}$). A few critical design steps are further described.

Step 1: Prescribe the k^2 and FBW_{S11} (or FBW_{S32}).

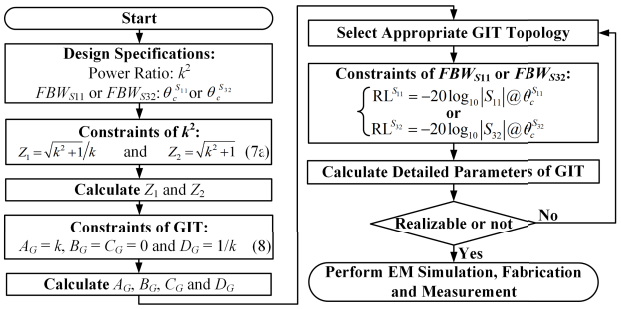

Fig. 2. Design flowchart for the proposed unequal PD.

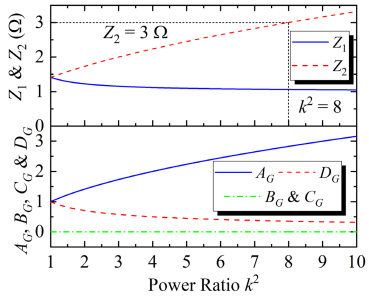

Fig. 3. Design chart of M_1, M_2, and GIT.

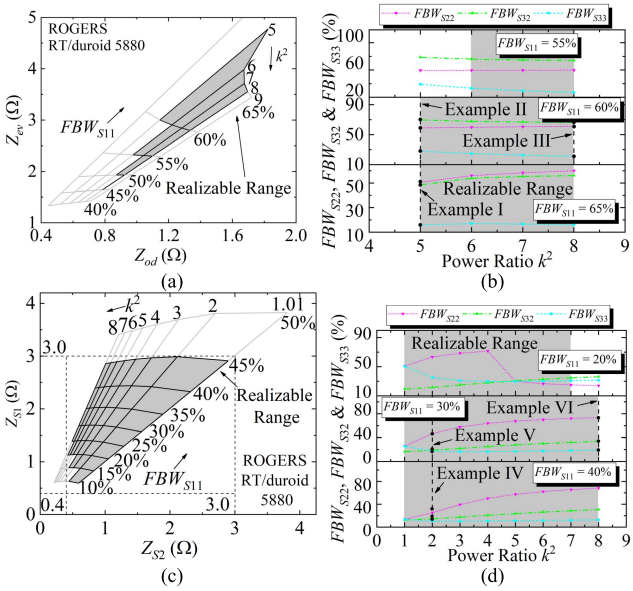

Fig. 4. Relationship among characteristic impedances, power ratio, and FBWs for two different cases. (a) Design chart of case I. (b) Realizable range of FBWs for case I. (c) Design chart of case II. (d) Realizable range of FBWs for case II.

Step 2: Based on the above-prescribed specifications, characteristic impedances (Z_1 and Z_2) and the *ABCD* matrix of GIT can be calculated from (7a) and (8), where their calculated results are shown in Fig. 3.

Step 3: According to the desired value of FBW_{S11} (or FBW_{S32}), appropriate GIT topology should be selected, where only cases I and II are considered for verification in this letter. By using the mathematical approach in [11], FBW_{S11} and FBW_{S32} can be calculated. The relationship among characteristic impedances, power ratio, and FBWs is shown in Fig. 4.

Step 4: Considering realization, a suitable substrate (Rogers RT/5880) is selected for fabrication. Then, the realizable range (gray range) can be easily drawn in Fig. 4.

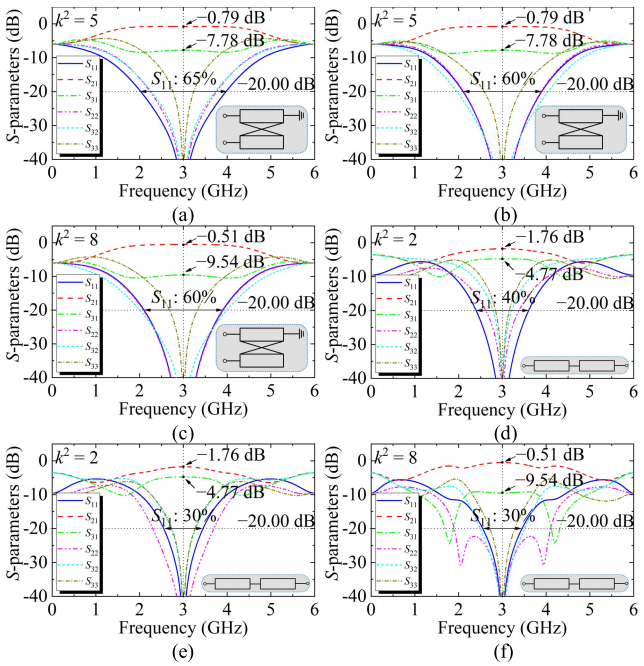

Fig. 5. Circuit-simulated results of six selected examples. (a) Example I: $Z_1 = 1.0955\ \Omega$, $Z_2 = 2.4495\ \Omega$, $Z_{ev} = 4.7758\ \Omega$, and $Z_{od} = 1.8242\ \Omega$. (b) Example II: $Z_1 = 1.0955\ \Omega$, $Z_2 = 2.4495$, $Z_{ev} = 2.9984\ \Omega$, and $Z_{od} = 1.1453\ \Omega$. (c) Example III: $Z_1 = 1.0607\ \Omega$, $Z_2 = 3.0000\ \Omega$, $Z_{ev} = 2.7969\ \Omega$, and $Z_{od} = 1.3358\ \Omega$. (d) Example IV: $Z_1 = 1.2247\ \Omega$, $Z_2 = 1.7321\ \Omega$, $Z_{S1} = 2.4213\ \Omega$, and $Z_{S2} = 1.7121\ \Omega$. (e) Example V: $Z_1 = 1.2247\ \Omega$, $Z_2 = 1.7321\ \Omega$, $Z_{S1} = 1.6558\ \Omega$, and $Z_{S2} = 1.1708\ \Omega$. (f) Example VI: $Z_1 = 1.0607\ \Omega$, $Z_2 = 3.0000\ \Omega$, $Z_{S1} = 1.6764\ \Omega$, and $Z_{S2} = 0.5927\ \Omega$.

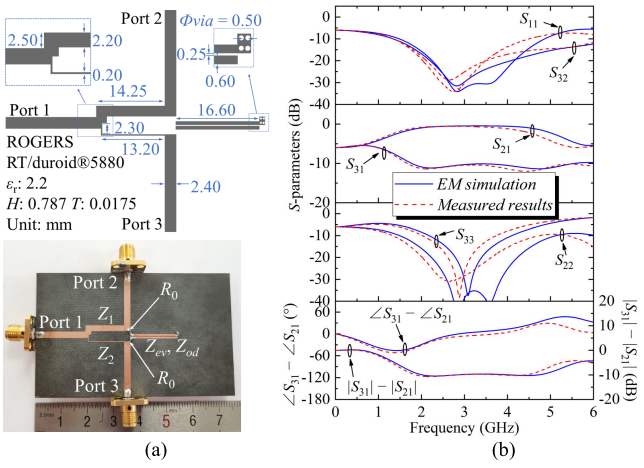

Fig. 6. Layout, photograph, simulated, and measured results of the proposed unequal PD (example III). (a) Layout and photograph of the proposed unequal PD. (b) Simulated and measured results of the proposed PD.

Step 5: Perform EM simulation and further slightly adjust the physical dimensions toward optimized target if necessary.

Based on Fig. 4, six design examples are also selected for verification, and their circuit simulation results are shown in Fig. 5. Therefore, the realizable ranges of power ratio and FBW are $5 \le k^2 \le 8$, $45\% \le \text{FBW}_{S11} \le 65\%$ in case I, and $1 < k^2 \le 8$, $10\% \le \text{FBW}_{S11} \le 45\%$ in case II, respectively. To sum up, the following rules can be summarized.

1) For the proposed topology, two TLs (M_1 and M_2) and GIT can be designed and discussed independently.
2) By suitably selecting different GIT topologies, different power ratios and FBW ranges can be realized, where k^2 and FBW_{S11} (or FBW_{S32}) can be adjusted independently. Because of limited pages, tedious discussion and comparison of FBW_{S32} are omitted in this letter.
3) Considering high power ratio, wide FBW_{S11}, and compact circuit size, case I is preferred for easy fabrication. To the best of the author's knowledge, such kind of discussion has not been reported in the former works yet.

TABLE I

COMPARISON WITH OTHER REPORTED UNEQUAL PDS [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]

Type	Ref.	k^2	Size ($\lambda_g \times \lambda_g$)	*FBW* of S_{11} and S_{32} (%@dB)	*FIWPR**
WPDs with Extra transformer	[1]	5:1	-	-/-@-20	No
	[2]	2:1	0.17×0.33	-@-14/-@-20	No
	[3]	10:1	0.25×0.25	16@-10/16@-20	No
	[4]	2:1	0.25×0.17	15@-15/15@-25	No
Gysel unequal PDs	[5]	12:1	DSPSL*	150@-10/-@-24	No
		2:1	DSPSL*	125@-10/-@-26	
	[6]	2:1	0.25×0.50	40@-15/40@-15	No
	[7]	4:1	0.16×0.41	65@-15/65@-15	No
Unequal PDs with three standard 50 Ω ports	[8]	4:1	1.06×0.25	-@-15/-@-20	No
	[9]	2:1	0.27×0.27	20@-20/20@-20	No
		4:1	0.24×0.24		
	[10]	2:1	0.25×0.20	15@-20/15@-20	No
		4:1	0.25×0.21		
		9:1	0.25×0.22		
	TW	**8:1**	**0.50×0.09**	**105@-10/155@-10 70@-15/95@-15 48@-20/46@-20**	**Yes**

DSPSL*: Double-Sided Parallel-Strip Line. TW: This Work.
*FIWPR**: FBW_{S11} (or FBW_{S32}) independent with k^2

IV. EXPERIMENTAL VERIFICATION

In practical implementation, one prototype circuit (example III) is selected for fabrication on Rogers RT/5880 substrate at $f_0 = 3$ GHz. Fig. 6(a) shows the layout and photograph of the proposed unequal PD, and Fig. 6(b) shows the results from the full-wave simulations (Sonnet) and measurements, where the resistances of two chip resistors are $R_0 = 51\ \Omega$. The simulated and measured results have matched very well with each other. Finally, a comparison with the former works [1], [2], [3], [4], [5], [6], [7], [8], [9], [10] is tabulated in Table I. Compared with WPDs and Gysel PDs, PDs with three standard 50-Ω ports are developed as inquired in applications. It is obvious that the proposed work could achieve high power ratio ($k^2 = 8$) with very compact circuit size ($0.50\lambda_g \times 0.09\lambda_g$). Because FBW_{S11} (or FBW_{S32}) and power ratio (k^2) can be adjusted independently, the measured FBW_{S11} exceeds 48%.

V. CONCLUSION

In this letter, a compact unequal PD with a GIT has been presented and designed. The design equations and examples have been given, compared, and discussed under different power ratios k^2 and bandwidths. For verification, one PD prototype has been fabricated to evidently validate the simulated results in the experiment.

REFERENCES

[1] J.-X. Chen and Q. Xue, "Novel 5:1 unequal Wilkinson power divider using offset double-sided parallel-strip lines," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 175–177, Mar. 2007.

[2] Y. L. Wu, H. Zhou, Y. X. Zhang, and Y. A. Liu, "An unequal Wilkinson power divider for a frequency and its first harmonic," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 11, pp. 737–739, Nov. 2008.

[3] B. Li, X. Wu, and W. Wu, "A 10:1 unequal Wilkinson power divider using coupled lines with two shorts," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 12, pp. 789–791, Dec. 2009.

[4] W.-C. Ip and K.-K. M. Cheng, "A novel unequal power divider design with dual-harmonic rejection and simple structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 4, pp. 182–184, Apr. 2011.

[5] L. Chiu and Q. Xue, "A parallel-strip ring power divider with high isolation and arbitrary power-dividing ratio," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 11, pp. 2419–2426, Nov. 2007.

[6] Y. Wu, Y. Liu, and S. Li, "A modified Gysel power divider of arbitrary power ratio and real terminated impedances," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 11, pp. 601–603, Nov. 2011.

[7] X. Wang, K.-L. Wu, and W.-Y. Yin, "A compact Gysel power divider with unequal power-dividing ratio using one resistor," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 7, pp. 1480–1486, Jul. 2014.

[8] Y.-Z. Zhu, X.-J. Zhang, X.-F. Wu, C. Li, and G.-Y. Fang, "Novel Wilkinson power divider with uniform impedance line," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, Dec. 2008, pp. 1–4.

[9] K.-K. M. Cheng and P.-W. Li, "A novel power-divider design with unequal power-dividing ratio and simple layout," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 6, pp. 1589–1594, Jun. 2009.

[10] T. Qi, S. He, Z. Dai, and W. Shi, "Novel unequal dividing power divider with 50 Ω characteristic impedance lines," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 3, pp. 180–182, Mar. 2016.

[11] N. Zhang, X. Wang, L. Zhu, and G. Lu, "A wideband bandpass power divider with out-of-band multi-transmission zeros and controllable equal-ripple levels," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1178–1187, Feb. 2022.